NOTRE DAME UNIVERSITY BANGLADESH

VLSI Design Lab Report-06

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Course Title: VLSI Design Lab
Experiment Name: Stick Diagram of XOR Gate

Submitted by:

Name: Istiak Alam
ID: 0692230005101005
Batch: CSE-20

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Submitted to:

Nafisa Tabassum,
Lecturer, Dept. of CSE
Notre Dame University Bangladesh

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Abstract

This laboratory experiment presents the implementation of the stick diagram of an XOR gate using the Microwind2 layout design tool. The XOR gate was realized based on its Boolean expression and CMOS logic principles. A simplified stick diagram was developed using standard layer representations such as polysilicon, diffusion, and metal interconnections. The functionality of the design was verified through simulation, and the output waveform was analyzed to confirm correct logical behavior. The experiment provides a clear understanding of the relationship between Boolean functions, CMOS circuit design, and their physical layout representation in VLSI systems.

1 Introduction

In VLSI design, the transformation of logical circuits into physical layouts is an essential step in the design process. Stick diagrams serve as a simplified and technology-independent method for representing circuit layouts, allowing designers to visualize transistor placement and interconnections without focusing on exact dimensions.

The XOR gate is an important combinational logic circuit widely used in arithmetic and digital systems. Its implementation in CMOS requires careful arrangement of pull-up and pull-down networks. In this experiment, the XOR gate is designed using its Boolean expression and represented using a stick diagram in Microwind2. The study of this design helps in understanding layout organization, layer interaction, and efficient circuit realization in VLSI systems.

2 Objective

The objectives of this laboratory experiment are as follows:

- To understand the concept and importance of stick diagrams in VLSI layout design.
- To implement stick diagrams of basic CMOS logic gates using Microwind2.
- To represent transistor-level circuits using simplified, technology-independent layouts.
- To analyze the arrangement of polysilicon, diffusion, and metal layers in CMOS design.
- To develop a clear understanding of the relationship between schematic design and physical layout.

3 XOR Gate

An XOR (Exclusive-OR) gate is a combinational logic gate that produces a logic HIGH output when the inputs are different and a logic LOW output when the inputs are the same. It is commonly used in digital circuits for comparison, parity checking, and arithmetic operations.

Boolean Function

$$Y = (AB + A'B')'$$

Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Stick Diagram

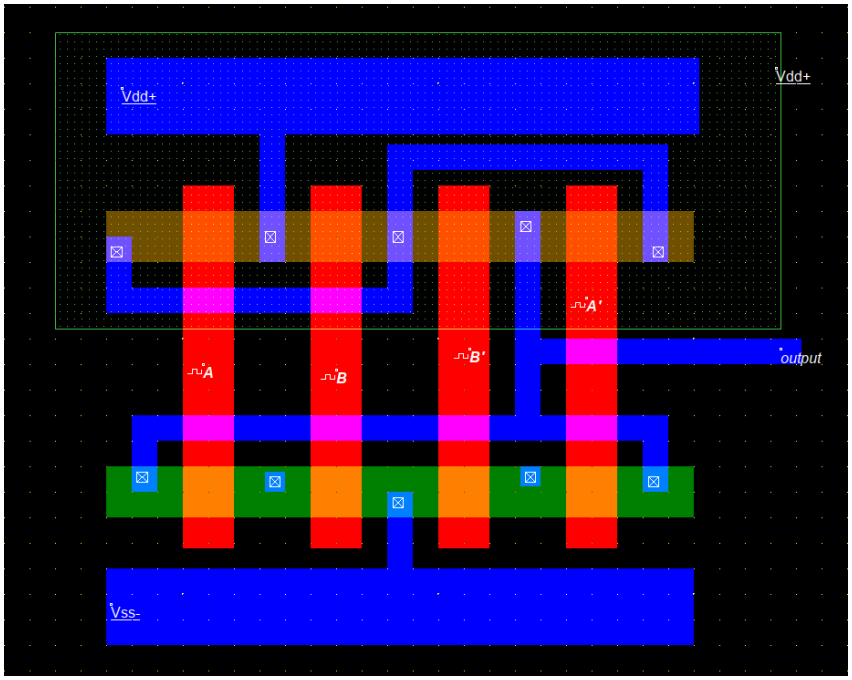

Figure 1: Stick Diagram of XOR Gate

Output

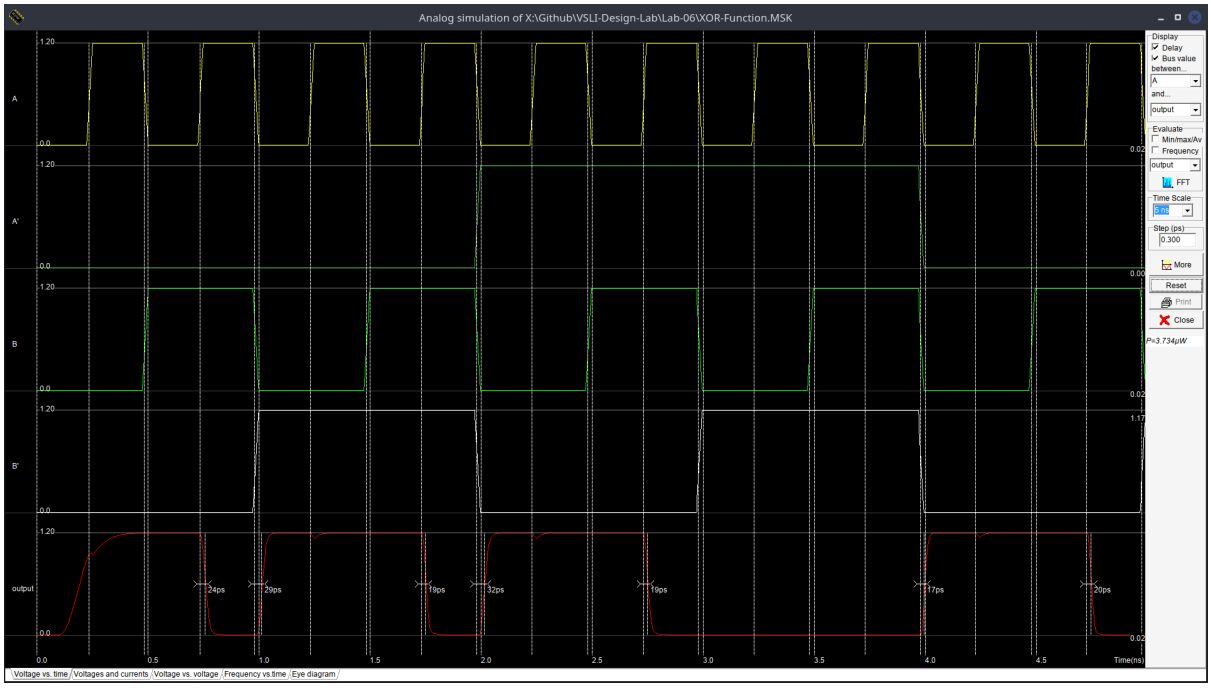

Figure 2: Output in Analog Simulation of XOR Gate

Observation

From the implementation and simulation of the XOR gate stick diagram using Microwind2, it was observed that the circuit produces a logic HIGH output when the inputs are different and a logic LOW output when both inputs are the same. The output waveform obtained from the simulation matches the theoretical truth table of the XOR function.

The stick diagram correctly represents the CMOS structure using appropriate placement of polysilicon, diffusion, and metal layers. Proper alignment and interconnection of these layers ensured correct signal flow and circuit operation. The simulation results confirm that the designed layout accurately implements the XOR logic function.

4 Conclusion

In this laboratory experiment, the stick diagram of an XOR gate was successfully designed and implemented using Microwind2. The experiment demonstrated how a Boolean expression can be translated into a CMOS-based layout representation using simplified stick diagram techniques.

The simulation results verified that the implemented design functions correctly according to the XOR truth table. This experiment enhanced the understanding of CMOS layout design, layer organization, and the relationship between logical design and physical implementation. The knowledge gained from this lab is essential for advanced VLSI design and layout optimization.